



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/584,484	05/07/2007	Karl Brander	2003P18385	3058
24131	7590	10/13/2010	EXAMINER	
LERNER GREENBERG STEMER LLP			LAM, ANN Y	
P O BOX 2480			ART UNIT	PAPER NUMBER
HOLLYWOOD, FL 33022-2480			1641	
MAIL DATE		DELIVERY MODE		
10/13/2010		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/584,484	Applicant(s) BRANDER ET AL.
	Examiner ANN Y. LAM	Art Unit 1641

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 30 July 2010.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-7,9-13 and 17-19 is/are pending in the application.
 4a) Of the above claim(s) 13 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-7,9-12 and 17-19 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 6/23/06, 3/8/10 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____
 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-7, 9-12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. 20030207326 (hereinafter "Su"), in view of U.S. 6,875,671 (hereinafter "Faris").

Su discloses nanopores 255, 330 which comprise single ion channels in lipid bilayer membranes. An electric field applied to proteins 230, 310 can cause these molecules to move through ion channels in lipid bilayer membranes. Ion channels may be incorporated into chips and operably coupled to detectors 257, 345. Paragraph 0072.

A chip containing the multiplanar structures may be divided into two or more parts. A layer of resist may be coated on the sides of each chip part, perpendicular to the conducting and insulating layers. An AFM/STP tip may be used to etch 5-10 nm lines in the resist layer overlaying each structure. Chemical etching may be used to create nano-scale grooves in each of the structures. When the chip parts are aligned and fused together, the grooves form nanopores 255, 330 and/or nanochannels 255, 330 which extend through the sensor layers 212, 323. Nanowires connecting the

conducting layers 327 to electrical detectors 345 may be formed by known methods discussed above. The nanowires may be used to apply a voltage across the conducting layers 327. Changes in current, resistance and/or other electrical properties may be detected with the passage of a protein 230, 310 labeled with electrically conductive labels 315, like gold nanoparticles 315, through the nanopore 255, 330. In certain embodiments of the invention, a thin layer of insulating material may be formed on the sides of the divided chip prior to lithography and etching to prevent current flow except through the nanopore 255, 330. Paragraph 0095.

Thus, as to claim 1, Su discloses at least two planar structures with grooves that when aligned form nanopores. One planar structure is equivalent to the claimed nanopore substrate, and one planar structure is equivalent to the claimed planar support layer. The resulting nanopore has a lipid bilayer, as disclosed in paragraph 0072, which is equivalent to the claimed biologically effective layer that is a biomembrane.

However, Su does not disclose alignment markings on one of the planar structures. However, the desirability of alignment markings for the benefit of precise positioning would have been obvious to the skilled artisan, and thus the skilled artisan would look to the prior art such as Faris for teachings on use of alignment markings to align to structures in the making of a device.

Specifically, Faris teaches improved alignment techniques, particularly for use with the device layer formation, removal and stacking methods. Column 5, lines 28-31.

Faris describes in one embodiment that layer one includes one or more alignment markings. These alignment markings may be etched regions, materials applied to the layer, shaped regions, or other known alignment markings. When polarized or unpolarized light is transmitted toward the polarizing reflector, light reflects from these alignment markings, and, in certain embodiments, back through the quarter wave phase retarder and subsequently through the polarizing reflector to project an image of the positions of the alignment marks. Column 33, lines 52-60.

The image of the position of the alignment markings is compared with an alignment reference. This alignment reference includes alignment marks that correspond to the alignment marks on the first layer. If the first layer is properly aligned, as determined, for example, by a comparator, no further action is required. However, in the event that the layer is not aligned, light will pass through the alignment reference can be detected by a comparator or a detector, and an appropriate X-Y-theta subsystem system will serve to reposition the first layer in the x direction, the y direction, and/or the angular direction until the alignment markings in the alignment reference from the reflected light reflected through the polarizing reflector are aligned. When the detector detects a null value (i.e., the light from the first layer in alignment with the alignment markings on the alignment reference) the layers are aligned.

Column 33, line 61 to column 34, line 9.

It is also disclosed that various products and devices may be formed using the processes disclosed. As mentioned above, "blanks", both as single layer and vertically integrated layers (complete with interconnections and optional

addressing and encoding functionality), generally of identical layers. Another series of products and devices may be formed from different layers. These may be standard (e.g., MEMs or microfluidics with integrated processors and/or memory). Column 40, lines 51-61.

General discussions of microfluidics is made, including its use in biotechnology and chemical analysis, Column 41, lines 34-40.

It is specifically disclosed that microfluidic devices may also be formed by stacking channels. In addition to stacking of channels, other microfluidic devices may be readily integrated. These devices may include flow sensors, microvalves and micropumps, etc. Column 41, line 46 to column 42, line 4.

Thus, while Su is silent as to use of alignment markings to align the grooves of the planar layers to form the nanopores, the skilled artisan would have appreciated techniques that facilitate the alignment procedure, and thus would have looked to the art such as the Faris patent which teaches a method for improving the alignment of layers in the fabrication of a micro-scale device. Given the suggestion by Faris that the disclosed techniques can be used to stack channels or other microfluidic devices, the skilled artisan would have had reasonable expectation of success in utilizing etched alignment markings and the alignment technique taught by Faris to align the grooves of the Su device.

As to claims 2 and 3, Su teaches that the surfaces of nanopores 255, 330, nanotubes 255, 330 or nanochannels 255, 330 may be modified by coating, for example to transform a surface from a hydrophobic to a hydrophilic surface and/or to

decrease adsorption of polymers such as proteins 230, 310 to a surface. Surface modification of common chip materials such as glass, silicon and/or quartz is known in the art (e.g., U.S. Pat. No. 6,263,286). Such modifications may include, but are not limited to, coating with silanes with various functional groups such as polyethyleneoxide or acrylamide, or any other known coating. Such coatings may not be appropriate where they would interfere with label 235, 245, 315 detection, such as interfering with electrical conductivity using an electrical detector 345. Paragraph 0064.

Moreover, as to claim 3, while it is not specifically disclosed that one layer is silicon oxide and one layer is silicon and carbon containing materials or glass, Su does disclose that common chip materials include glass and silicon and that surface modification of such common chip materials is known, as discussed immediately above. The choice of particular material for the planar layers as claimed falls within the common types of chip materials disclosed by Su and thus appear to be predictable choices.

As to claim 4, it is noted that Su further teaches the following.

In some embodiments, nanopores 255, 330, sensor layers 212, 323 and other components of the disclosed apparatus 100 may be incorporated into one or more Micro-Electro-Mechanical Systems (MEMS). MEMS are integrated systems that may comprise mechanical elements, actuator elements, control elements, detector 257, 345 elements and/or electronic elements. All of the components may be manufactured by known microfabrication techniques on a common chip, comprising a silicon-based or equivalent substrate. Paragraph 0074.

The electronic components of MEMS may be fabricated using integrated circuit (IC) processes (e.g., CMOS, Bipolar, or BICMOS processes). They may be patterned using photolithographic and etching methods known for semiconductor chip manufacture. The micromechanical components may be fabricated using "micromachining" processes that selectively etch away parts of the silicon wafer and/or add new structural layers to form the mechanical and/or electromechanical components. Basic techniques in MEMS manufacture include depositing thin films of material on a substrate, applying a patterned mask on top of the films by photolithographic imaging or other known lithographic methods, and selectively etching the films. A thin film may have a thickness in the range of a few nanometers to 100 micrometers. Deposition techniques of use may include chemical procedures such as chemical vapor deposition (CVD), electrodeposition, epitaxy and thermal oxidation and physical procedures like physical vapor deposition (PVD) and casting. Sensor layers 212, 323, of 5 nm thickness or less may be formed by such known techniques. Standard lithography techniques may be used to create sensor layers 212, 323 of micron or sub-micron dimensions, operably coupled to detectors 257, 345 and nanopores 255, 330. Paragraph 0075.

It is also noted that Su defines the terms "nanopore" 255, 330, "nanochannel" 255, 330 and "nanotube" 255, 330 to refer respectively to a hole, channel or tube with a diameter or width of between 1 and 999 nanometers (nm), more typically between 1 and 100 nm, even more typically between 1 and 10 nm. Paragraph 0015.

Thus, as to claims 4 and 17, while Su is silent as to the thickness of the substrate and diameter of the nanopores having an aspect ratio in the range claimed, such choice appears to fall within workable ranges, given the dimensions disclosed by Su and the versatility in forming the device as described by Su.

As to claims 5 and 18, the claimed range in diameter of the nanopores falls within the disclosed range of diameter of the nanopores in paragraph 0015.

As to claims 6, 7 and 19, Su discloses the following. It is disclosed that fabrication of nanopores 255, 330, nanotubes 255, 330 and/or nanochannels 255, 330, individually or in arrays, may utilize any technique known in the art for nanoscale manufacturing. In certain embodiments of the invention, nanopores 255, 330, nanochannels 255, 330 and/or nanotubes 255, 330 may be constructed on a solid-state matrix comprising sensor layers 212, 323 using known nanolithography methods, including but not limited to chemical vapor deposition, electrochemical deposition, chemical deposition, electroplating, thermal diffusion and evaporation, physical vapor deposition, sol-gel deposition, focused electron beam, focused ion beam, molecular beam epitaxy, dip-pen nanolithography, reactive-ion beam etching, chemically assisted ion beam etching, microwave assisted plasma etching, electro-oxidation, scanning probe methods, chemical etching, laser ablation, or any other method known in the art. Paragraph 0057.

Thus, as to claims 6, 7 and 19, Su discloses that the nanopores may be formed in an array. While Su is silent as to the area in which the array section is provided, or the distance between the nanopores, the skilled artisan would have recognized that the

Su invention is not limited a particular size limitation or density limitation. The ranges of array section and distance between the nanopores as claimed fall within workable ranges of the Su invention, and thus their choices would have been within the skills of the ordinary artisan.

As to claim 9, while Su is silent as to whether the lipid bilayer is from a natural or non-natural source, the skilled artisan would have recognized that the Su invention is not limited to use of a bilayer that is from a natural or non-natural source. It would have been predictable by the skilled artisan that either source of the bilayer would be useful in the assay device, as may be desirable by the skilled artisan in a particular type of assay.

As to claim 10, Su discloses that the ion channels in the lipid bilayer membranes of the nanopores may include, but are not limited to, *Staphylococcus aureus* alpha-hemolysin and/or mitochondrial voltage-dependent anion channels. These ion channels may remain open for extended periods of time. An electric field applied to proteins 230, 310 can cause these molecules to move through ion channels in lipid bilayer membranes. Ion channels may be incorporated into chips and operably coupled to detectors 257, 345. Paragraph 0072. While Su does not discloses that the lipid bilayer membranes hosts a non-lipid molecule that is a synthetic compound, the disclosure explicitly states that the exemplary ion channels are not limiting. It is predictable by the skilled artisan that ion channels may be synthetic or provided otherwise, as such would provide alternative ion channels for a similar analytical purpose.

As to claim 11, the ion channels disclosed by Su in paragraph 0072 include a non-lipid functional molecule. (It is noted that the recitation of recombinant DNA and RNA technologies refers to a method of making and that the present claims are directed to a device or product. Thus since the prior art meets the structural limitations of the claims, then it meets the claims.)

As to claim 12, while Su is silent as to whether the lipid bilayer is made from at least one intact living cell, the skilled artisan would have recognized that the Su invention is not limited to a particular type of lipid bilayer, and thus envisions encompassing a bilayer that is made from an intact living cell, as is also suggested by the particular types of ion channels exemplified in paragraph 0072.

Response to Arguments

Applicant's arguments with respect to the above rejected claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendments adding the limitation regarding the alignment marks and the nanopores of the support layer being aligned with the nanopores of the substrate have overcome the Lee reference because the substrate of the Lee reference is only disclosed as porous, and thus there lacks a reason for aligning the openings of the porous substrate (12) with the nanopores of the layer (14).

A new rejection has been made however in light of the amendments.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANN Y. LAM whose telephone number is (571)272-0822. The examiner can normally be reached on Mon.-Thurs. 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Shibuya can be reached on 571-272-0806. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ann Y. Lam/
Primary Examiner, Art Unit 1641